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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/669,354 | 09/26/2000 | Hisanobu Ishiyama | 81751.0009 | 4577 |

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| EXAMINER |
|---|
| NGUYEN, HAU H |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2676 | 11 |

DATE MAILED: 08/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/669,354 | ISHIYAMA, HISANOBU | |
| | Examiner | Art Unit | |
| | Hau H Nguyen | 2676 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6,7* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2, 4-8, 12, and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Shimizu (U.S. Patent No. 5,801,674).

Referring to claims 1, 4-7, and 18 Shimizu teaches a display device comprising a liquid crystal display panel having a plurality of scanning electrodes (second electrodes), a plurality of signal electrodes divided into a plurality of signal electrode groups (first electrodes), and liquid crystal elements arranged at intersections of the scanning electrodes and the signal electrodes; a controller (an external MPU) for outputting control signals including a start signal, enable signal and clock signal and display data; and a plurality of drivers supplied with the display data and the control signals including the start signal, enable signal and clock signal from the controller, for fetching the display data and selectively supplying the fetched display data to the plurality of signal electrode groups (col. 2, lines 40-52). As shown in Fig. 1, the LCD display device as taught by Shimizu comprises a Y driver 2 (second driver) for driving the scanning electrodes and four X drivers 3, 4, 5, 6 (first driver) for driving four signal electrode groups obtained by dividing all of the horizontal signal electrodes in a horizontal direction are arranged in the peripheral portion of the LCD panel 1 (col. 3, lines 53-57). Shown in Fig. 2 is the internal

structure of a single IC X driver 3 (master IC), wherein the data fetch starting signal and load signal are generated in the cascade connection control circuit 12 (a display control signal generation section) by decoding the SYNC signal (col. 4, lines 61-64). Each of the IC X driver has an input terminal EI together with the input circuit 11 for receiving control signals, and output terminal EO for generating control signal to the next-stage X driver (col. 4, lines 1-10) through external wiring as shown in Fig. 1. Shimizu further teaches the operation of each of the X drivers is interrupted when the operation of fetching the display data for driving the signal electrode group connected to the X driver is completed. At this time, the X driver outputs an enable output for driving the next-stage X driver from the EO terminal thereof. Thus, each of the X drivers starts to fetch data when the operation of the preceding-stage X driver is ended, and the operation thereof is effected for a period of time necessary for fetching data and then terminated. When all of the X drivers 3 to 6 have fetched data allotted to the respective X drivers, display signals of one horizontal period H for driving the signal electrodes are simultaneously output to the LCD panel 1 from the respective drivers 3 to 6 in response to the LOAD signal contained in the control signal SYNC from the controller 7 (col. 4, lines 4-18). Therefore, it is implied that an internal delay circuit holds data until all data have been fetched and loaded to display, and the output enable signal for the next stage driver is output before display control signal passes through the internal circuit. Since the display control signals are difference from each of the X drivers 3-6, time delay in each driver is different from one another.

In regard to claims 2 and 16, as shown in Fig. 2, Shimizu teaches a data register 15 (display memory), an LCD driving circuit 17 (driver). As shown in Figs. 4A and 4B, based on

the clock signal A, SYNC signal B (display control signal), data is latched into flip-flops 111-11n for displaying according to their addresses in each of X drivers IC1-IC4 (col. 7, lines 5-14).

In regard to claims 8 and 12, as cited and as shown in Fig. 2, Shimizu teaches an interface circuit 11 coupled to receive control signal from external controller 7 (Fig. 1), address circuit 16, display memory 15, display control signal 12, LCD driver 17, input terminal EI, output terminal EO. Shimizu further teaches the enable output of "1" (display control enabled) (to the next-stage X driver 4) is derived from the EO terminal of the first-stage X driver 3. Since the EI' signal is "0" in the other X drivers 4 to 6, the enable output is kept at "0" (disabled) (col. 8, lines 19-22).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu (U.S. Patent No. 5,801,674) in view of Yasunishi (U.S. Patent No. 6,094,243).

Referring to claims 3 and 17, as cited above, Shimizu teaches all the limitations of claim 3, except for the display control includes grayscale control pulse for generating pulse width modulation signal.

However, Yasunishi teaches a method for driving a matrix-type liquid crystal display device capable of conducting a gray-scale display, wherein as shown in Fig. 11, comprising

pulse width control circuit 21 for outputting various control signals indicated by S250 for controlling the operation of the display data transformation circuit 1".

Therefore, it would have been obvious to one skilled in the art to utilize the method of providing gray-scale control as taught by Yasunishi in combination with the method of driving LCD device as taught by Shimizu in order to suppress flickers in the displayed images which would occur in the frame modulation method and suppress the display non-uniformity which would occur in the pulse width modulation method (col. 7, lines 12-19).

5. Claims 9-11, 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu (U.S. Patent No. 5,801,674) in view of S-MOS System, Inc., Dot Matrix LCD Driver SED 1520/21 Version 1.0 (October, 1996) (hereinafter S-MOS)

Referring to claims 9 and 13, as cited above, Shimizu teaches a selection circuit for enabling the next stage slave X driver 4 output from the master X driver 3 through the EO output terminal. Thus, Shimizu teaches all the limitations of claims 9 and 13, except that input/output capable of switching from outputting display control to inputting display control.

However, S-MOS teach a method for driving LCD, comprising a plurality of ICs, which can be configured to be a master IC or a slave IC as shown on page 15. In the table shown on page 22, the input/output switching state configuration is based on the control signal FR and the selection signal M/S for selecting master or slave state.

Therefore, it would have been obvious to one skilled in the art to utilize the teachings of S-MOS in combination with the method as taught by Shimizu in order to permit the user to implement high-performance handy systems operating from a miniature battery (page 5).

Referring to claims 10-11 and 14-15, although Shimizu does not teach using an AND or an OR gate for selecting master or slave IC. However, with reference again to the table on page 22, section 3.2.3.2 of the manual for driver SED 1520/21, the state of the driver (master or slave) depends on both the M/S signal and FR signal. Therefore, it is implied a combinational logic function using either AND or OR circuit to connect these two signals in order to switch the state of the IC.

Therefore, it would have been obvious to one skilled in the art to utilize the teachings of S-MOS in combination with the method as taught by Shimizu in order to permit the user to implement high-performance handy systems operating from a miniature battery (page 5).

***Conclusion***

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

08/05/2003

Matthew C. Bella

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
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